Listing of the Claims:

The following claims are currently pending in the present application.

1-49. (Cancelled)

50. (Previously presented) A method of operating a memory device, the memory device having addressing and data path circuitry for reading data and providing the same to external terminals of the memory device, the method comprising:

providing a memory command and a memory address to the memory device;

in response to a first memory command, providing memory data from a memory location in a memory array corresponding to the memory address to the external terminals of the memory device via a data path; and

in response to a second memory command, reading parameter data stored in a first format from a parameter memory corresponding to the memory address, processing the parameter data in the first format to generate parameter data in a second format, and decoupling the data path from the memory array and coupling the same to receive the parameter data in the second format and provide the parameter data to the external terminals of the memory device.

51. (Previously presented) The method of claim 50 wherein processing the parameter data in the first format to generate parameter data in a second format comprises adding null bits to the parameter data until it has the same number of bits of the memory data.

52. (Previously presented) The method of claim 51 wherein the number of bits of the memory data is 16-bits.

53. (Previously presented) The method of claim 50 wherein reading parameter data stored in a first format comprises:

providing the memory address as a register address to an register address decoder; and

reading parameter data from a location in a register corresponding to the register address.

54. (Previously presented) The method of claim 53, further comprising:

generating a control signal in response to the second memory command;

activating a register driver coupled to the register and disabling sense amplifier circuits coupled to the memory array in response to the control signal.

55. (Previously presented) The method of claim 50 wherein processing the parameter data in the first format to generate parameter data in a second format comprises converting the parameter data to the same format in which data from the memory data is transmitted.

56. (Previously presented) The method of claim 50 wherein the parameter data comprises a plurality of data bits representing clock speed information of the memory device.

57. (Previously presented) The method of claim 56, further comprising operating the memory device at a clock speed based on the clock speed information.

58. (Previously presented) A method of operating a memory device, the memory device having addressing and data path circuitry for reading data and providing the same to external terminals of the memory device, the method comprising:

providing a memory command requested data and a memory address to the memory device;

in response to receiving the memory command having an inactive command bit, accessing a memory location in a memory array corresponding to the memory address and coupling a data path to the memory array to provide the memory data stored at the memory location to the external terminals; and

in response to a memory command having an active command bit, accessing a parameter storage location corresponding to the memory address to read parameter data stored therein, reformatting the parameter data, and coupling the data path to the parameter storage location to provide the reformatted parameter data to the external terminals.

59. (Previously presented) The method of claim 58 wherein reformatting the parameter data comprises converting the parameter data to the same format in which data from the memory data is provided.

60. (Previously presented) The method of claim 59 wherein converting the parameter data comprises adding null bits to the parameter data until it has the same number of bits of the memory data.

61. (Previously presented) The method of claim 60 wherein the number of bits of the memory data is 16-bits.

62. (Previously presented) The method of claim 58 wherein accessing the parameter storage location comprises:

providing the memory address as a register address to an register address decoder; and

reading parameter data from a location in a register corresponding to the register address.

63. (Previously presented) The method of claim 62, further comprising:

generating a control signal in response to the memory command having the inactive command bit;

activating a register driver coupled to the register and disabling sense amplifier circuits coupled to the memory array in response to the control signal.

64. (Previously presented) The method of claim 58 wherein the parameter data comprises a plurality of data bits representing clock speed information of the memory device.

65. (Previously presented) The method of claim 64, further comprising operating the memory device at a clock speed based on the clock speed information.

66. (Previously presented) A method for reading data from a memory device having external data terminals, the method comprising:

storing parameter data for the memory device in a parameter storage location, the parameter data having a first data format;

storing memory data in a memory array, the memory data having a second data format;

receiving a memory command having command signals and memory address signals;

decoding the command and memory address signals;

accessing the parameter data stored in the parameter storage location corresponding to memory address signals, reformatting the parameter data from the first data format to the second data format, and coupling the reformatted parameter data to the external data terminals in response to the command including an active parameter read signal; and

accessing the memory data stored in the memory array corresponding to the memory address signals and coupling the memory data to the external data terminals in response to the command including an inactive parameter read signal.

67. (Previously presented) The method of claim 66 wherein reformatting the parameter data from the first data format to the second data format comprises adding null bits to the parameter data until it has the same number of bits of the memory data.

68. (Previously presented) The method of claim 67 wherein the number of bits of the memory data is 16-bits.

69. (Previously presented) The method of claim 66 wherein accessing the parameter data stored in the parameter storage location comprises:

providing the memory address signals as a register address to an register address decoder; and

reading the parameter data from a location in a register corresponding to the register address.

70. (Previously presented) The method of claim 69, further comprising:

generating a control signal in response to the command including an active parameter read signal; and

activating a register driver coupled to the register and disabling sense amplifier circuits coupled to the memory array in response to the control signal.

71. (Previously presented) The method of claim 66 wherein storing the parameter data comprises storing a plurality of data bits representing clock speed information of the memory device.

72. (Previously presented) The method of claim 71, further comprising operating the memory device at a clock speed based on the clock speed information.

73. (Previously presented) A method of operating a memory device having command and address terminals, the method comprising:

receiving address signals at the address terminals;

receiving command signals at the command terminals;

decoding the command signals and determining whether a parameter read command has been requested;

in the event a parameter read command is received, accessing a parameter storage location corresponding to the address signals to retrieve parameter data, reformatting the parameter data to an output data format, and coupling the reformatted parameter data to a data path; and

in the event a memory read command is not received, decoding the address signals, accessing a memory location in a memory array corresponding to the address signals to retrieve memory data and coupling the memory data to the data path if a parameter read command is not received to provide the memory data in the output data format.

74. (Previously presented) The method of claim 73 wherein reformatting the parameter data to an output format comprises adding null bits to the parameter data until it has the same number of bits of the memory data.

75. (Previously presented) The method of claim 74 wherein the number of bits of the memory data is 16-bits.

76. (Previously presented) The method of claim 73 wherein accessing the parameter data storage location comprises:

providing the memory address signals as a register address to an register address decoder; and

reading the parameter data from a location in a register corresponding to the register address.

77. (Previously presented) The method of claim 76, further comprising:

generating a control signal in response to the command including an active parameter read signal; and

activating a register driver coupled to the register and disabling sense amplifier circuits coupled to the memory array in response to the control signal.

78. (Previously presented) The method of claim 73 wherein the parameter data comprises a plurality of data bits representing clock speed information of the memory device.

79. (Previously presented) The method of claim 78, further comprising operating the memory device at a clock speed based on the clock speed information.